having a non-planar surface. Furthermore, a planar T-RAM structure is easier to fabricate, since the depth of focus for the lithographic tools and metal interconnects is easier to handle than the three-dimensional vertical device of the prior art T-RAM structure.

To the contrary, Nemati is directed to a combination of a horizontal gate device (Fig. 1, #12) and a vertical thyristor device (Fig. 1, #10). Thus Nemati also teaches away from a planar structure by having devices of dissimilar heights that when combined create a non-planar structure. Takeguchi is directed to a flash memory array including a floating gate (Fig. 3, #24) that results in a structure with a non-planar surface. Thus, Takeguchi does not cure the defects of Nemati. Applicants submit that amended Claim 43 is patentable over Nemati, Takeguchi, or any combination thereof. By virtue of their dependency upon Claim 43, it is also submitted that amended Claims 44-46 and 51-53 are also patentable.

With reference to the 35 USC §103(a) rejection over Hsu, it is submitted that Hsu is not prior art, as stated under 35 U.S.C. §103(c), and also under MPEP §706.02(l)(1). That section of the statute states, in part:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed inventions were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The MPEP section states that the above-quoted 35 U.S.C. §103(c) applies to all utility, design and plant patent applications filed on or after November 29, 1999.

The present application was filed on January 26, 2001. Further, the present

application is assigned to International Business Machines Corporation, Armonk, NY, also the assignee of the Hsu application. In addition, the inventors for Hsu Patent Application are not identical to the inventors for the present application. Accordingly, it is submitted that the Hsu Patent Application is not prior art under 35 U.S.C. §103(c).

All of the claims pending in the Application are now believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

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Marked Up Version of the Specification

Please insert the following directly before the paragraph beginning on line 3 of page 8:

As is known to one of ordinary skill in the art, a transfer gate and thyristor each comprises at least one source, one drain, and one body. With reference to Figure 14, it is shown that transfer gate 230 and thyristor 240 each has a horizontal configuration. Thus, the horizontal configuration of transfer gate 230 includes a source, a drain, and a body located on a horizontal plane, wherein the horizontal plane is approximately parallel to the top surface of substrate 136. Moreover, the horizontal configuration of thyristor 240 includes a source, a drain, and a body located on a horizontal plane, wherein the horizontal plane is approximately parallel to the top surface of substrate 136.

Marked-Up Version of the Claims

43. (Once Amended) A memory system comprising a plurality of T-RAM memory cells arranged in an array, [each of the plurality of T-RAM cells comprising a thyristor portion having two halo regions having different polarities] wherein each of the plurality of T-RAM memory cells includes a first and a second horizontal device, said first and second horizontal device being approximately the same height, each of said first and second horizontal device having a planar top surface.

44. (Once Amended) The memory system as in Claim 43, wherein [each of the plurality of T-RAM cells further comprises a transfer gate portion] the first horizontal device is a thyristor and the second horizontal device is a transfer gate.

45. (Once Amended) The memory system as in Claim 44, wherein [each of] the transfer gate [portions of the plurality of T-RAM cells] comprises a halo region of

a single polarity.

46. (Once Amended) The memory system as in Claim 45, wherein the single polarity halo region of the transfer gate [portions of each of the plurality of T-RAM cells] is fabricated in the same steps as a [one of the] halo [regions] region of the thyristor [portion].

51. (Once Amended) The memory system as in Claim [50] 43, wherein the first [support] device is a p-MOS [support] device and the second [support] device is an n-MOS [support] device.

52. (Once Amended) The memory system as in Claim 51, wherein the p-MOS [support] device comprises an n-type halo region and the n-MOS [support] device comprises a p-type halo region.

53. (Once Amended) The memory system as in Claim 52, wherein the n-type halo region of the p-MOS [support] device is fabricated simultaneously with fabrication steps for fabrication of [one of the] a halo region [regions] of the T-RAM cells and the p-type halo region of the n-MOS [support] device is fabricated simultaneously with fabrication steps for fabrication of a second [the other] halo region of the T-RAM cells.